



Applicant	James Leroy Snell, et al.	<u>THIRD</u> <u>SUPPLEMENTAL</u> <u>PRELIMINARY</u> <u>AMENDMENT</u>
Serial No.	10/005,483	
Filing Date	November 9, 2001	
Group Art Unit	2631	
Examiner Name	Unknown	
Attorney Docket No.	125.003USR1	
Title: HIGH DATA RATE SPREAD SPECTRUM TRANSCEIVER AND ASSOCIATED METHODS		

Commissioner for Patents
Washington, DC 20231

Dear Sir:

Prior to initial review, please amend the above-identified reissue application as follows:

IN THE CLAIMS

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Please amend the claims as follows.

62. (Amended) A spread spectrum radio transceiver comprising:
a baseband processor and a radio circuit coupled thereto, said baseband processor
comprising
a demodulator for spread spectrum phase shift keying (PSK) demodulating
information received from said radio circuit,
at least one analog-to-digital (A/D) converter having an output coupled to said
demodulator and an input AC-coupled to said radio circuit,
said demodulator comprising at least one modified Walsh code function
correlator for decoding information according to a modified Walsh
code reducing an average DC signal component, and
a modulator for spread spectrum PSK modulating information for
transmission via the radio circuit, said modulator comprising at least
one modified Walsh code function encoder for encoding information

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according to the modified Walsh code.

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64. (Amended) A spread spectrum radio transceiver according to claim 63 wherein said modulator is configured to modulate data packets to include a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.

65. (Amended) A spread spectrum radio transceiver according to claim 64 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

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71. (Amended) A spread spectrum radio transceiver according to claim 62 wherein said at least one modified Walsh code function correlator comprises:

a modified Walsh function generator; and

a plurality of parallel coupled correlators coupled to said modified Walsh function generator.

72. (Amended) A spread spectrum radio transceiver according to claim 62 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is configured to generate a preamble; and wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.

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75. (Amended) A spread spectrum radio transceiver according to claim 62 wherein said radio circuit comprises:

a quadrature intermediate frequency modulator/demodulator coupled to said baseband processor; and

an up/down frequency converter coupled to said quadrature intermediate frequency modulator/demodulator.

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76. (Amended) A spread spectrum radio transceiver according to claim 75 wherein said radio circuit further comprises:

a low noise amplifier having an output coupled to an input of said up/down converter;
and
a radio frequency power amplifier having an input coupled to an output of said up/down converter.

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78. (Amended) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a demodulator for spread spectrum phase shift keying (PSK) demodulating;
at least one analog-to-digital (A/D) converter having an output coupled to said demodulator and an input AC-coupled to receive information;
said demodulator comprising at least one orthogonal code function correlator for decoding information according to an orthogonal code reducing an average DC signal component to thereby increase AC-coupling to said at least one A/D converter; and
a modulator for spread spectrum PSK modulating information for transmission, said modulator comprising at least one orthogonal code function encoder for encoding information according to the orthogonal code.

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80. (Amended) A baseband processor according to claim 79 wherein said modulator is configured to modulate data packets to include a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.

81. (Amended) A baseband processor according to claim 80 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

85. (Amended) A baseband processor according to claim 78 wherein said modulator is further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one orthogonal code function encoder.

86. (Amended) A baseband processor according to claim 78 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

87. (Amended) A baseband processor according to claim 78 wherein the orthogonal code is a bi-orthogonal code.

88. (Amended) A baseband processor according to claim 78 wherein said at least one orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

89. (Amended) A baseband processor according to claim 78 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is configured to generate a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

91. (Amended) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a modulator for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator comprising

at least one encoder for encoding information for transmission,

wherein said modulator is configured to operate in one of a first format defined by bi-

phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate, and

wherein said modulator is configured to modulate data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and

a demodulator for spread spectrum PSK demodulating received information, said demodulator comprising

at least one correlator for decoding received information,

wherein said demodulator is configured to operate in one of the first and second formats,

wherein said demodulator is configured to demodulate data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header,

a first carrier tracking loop for the third format, and

a second carrier tracking loop for the first and second formats.

92. (Amended) A baseband processor according to claim 91 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

95. (Amended) A baseband processor according to claim 91 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is further configured to generate a preamble; and wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.

97. (Amended) A modulator for a spread spectrum radio transceiver, said modulator configured to modulate information for transmission by spread spectrum phase shift keying (PSK), said modulator comprising at least one orthogonal code function encoder for encoding information according to an orthogonal code for reducing an average DC signal

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component.

99. (Amended) A modulator according to claim 98 wherein said modulator is configured to modulate data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats.

100. (Amended) A modulator according to claim 99 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

101. (Amended) A modulator according to claim 97 wherein said modulator is configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one orthogonal code function encoder, and wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

102. (Amended) A modulator according to claim 97 wherein said at least one orthogonal code function correlator comprises:

an orthogonal code function generator; and

a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

103. (Amended) A modulator according to claim 97 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

104. (Amended) A modulator according to claim 97 wherein the orthogonal code is a bi-orthogonal code.

105. (Amended) A demodulator for a spread spectrum radio transceiver, said demodulator configured to demodulate information for by spread spectrum phase shift keying (PSK) said demodulator for spread spectrum phase shift keying (PSK) demodulating information

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received from a radio circuit, said demodulator means comprising at least one orthogonal code function correlator for decoding information according to an orthogonal code reducing an average DC signal component.

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107. (Amended) A demodulator according to claim 106 wherein said demodulator is configured to demodulate data packets including a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats, and for switching to the respective one of the first and second formats of the variable data after the header.

108. (Amended) A demodulator according to claim 107 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

113. (Amended) A demodulator according to claim 105 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

114. (Amended) A demodulator according to claim 105 wherein the orthogonal code is a bi-orthogonal code.

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115. (Amended) A demodulator according to claim 105 wherein said at least one orthogonal code function correlator comprises:
an orthogonal code function generator; and
a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

116. (Amended) A method for baseband processor for spread spectrum radio communication, the method comprising:
spread spectrum phase shift keying (PSK) modulating information for transmission

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while encoding the information according to the orthogonal code for reducing an average DC signal component; and

spread spectrum PSK demodulating received information by decoding the received information according to the orthogonal code.

119. (Amended) A method according to claim 118 further comprising:
modulating data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and
demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

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120. (Amended) A method according to claim 119 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

121. (Amended) A method according to claim 116 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

122. (Amended) A method according to claim 116 wherein the orthogonal code is a bi-orthogonal code.